R E M A R K S

Reconsideration of this application, as amended, is respectfully requested.

THE CLAIMS

Independent claim 1 has been amended to clarify that the variable capacitor section comprises capacitors and switching elements that are connected to the capacitors in series, along the lines previously recited in (now canceled) claim 2. In addition, claim 1 has been amended to clarify that the memory is configured to store at least two items of data for setting a capacitance of the variable capacitor section to at least two suitable values that are suitable for receiving radio waves having at least two frequencies, along the lines previously recited in (now canceled) claim 6. Still further, claim 1 has been amended to clarify that the controller: (i) detects suitable combinations of on and off states of the switching elements such that the radio wave receiver is in a predetermined reception state for each of the at least two frequencies, (ii) writes into the memory data for setting the on and off states of the switching elements to the suitable combinations, (iii) reads the data from the memory in accordance with a received radio wave, and (iv) turns on and off the switching elements based on the read data.

Independent claim 11, moreover, has been amended in a similar manner to independent claim 1, and claims 3-5, 8-9, 13-15, and 18 have been amended to better accord with amended independent claims 1 and 11.

Still further, the claims have been amended to make some minor grammatical improvements and to correct some minor antecedent basis problems so as to put them in better form for issuance in a U.S. patent.

No new matter has been added, and it is respectfully requested that the amendments to the claims be approved and entered.

THE PRIOR ART REJECTIONS

Claims 1-7, 9-10 and 20-22 were rejected under 35 USC 103 as being obvious in view of the combination of USP 5,136,719 ("Gaskill et al") and US 2001/0036811 ("Kianush et al"); and claims 8 and 11-19 were rejected under 35 USC 103 as being obvious in view of the combination of Gaskill et al, Kianush et al and USP 4,315,332 ("Sakami et al"). These rejections, however, are respectfully traversed with respect to the claims as amended hereinabove.

According to the present invention as recited in amended independent claims 1 and 11, a variable capacitor section (201) is connected to an antenna and includes capacitors (C1 to Cn,

Cex1, Cex2) and switching elements (T1 to Tn, Tex1, Tex2) connected to the capacitors in series. A memory (2701) is configured to store at least two items of data for setting a capacitance of the variable capacitor section to at least two suitable values that are suitable for receiving radio waves having at least two frequencies. And a controller (206) is configured to (i) detect suitable combinations of on and off states of the switching elements such that the radio wave receiver is in a predetermined reception state for each of the at least two frequencies, (ii) write into the memory data for setting the on and off states of the switching elements to the suitable combinations, (iii) read the data from the memory in accordance with a received radio wave, and (iv) turn on and off the switching elements based on the read data. That is, the present invention as recited in amended independent claims 1 and 11 provides a radio wave receiver for at least two frequencies.

Gaskill et al, by contrast, discloses a tuning mode operation in which the control circuit 16 sweeps the varactor biasing voltage over its full range and determines which bias voltage yields the maximum received signal strength. The sweeping is accomplished by a clock 38, a sequencer 40 and a digital-to-analog (D/A) converter 42. The clock 38, which may operate at 25 kilohertz, for example, steps the sequencer 40 through a plurality of states. In the illustrated embodiment,

the sequencer may have 100 states, each one providing a successively larger 8 bit 5 binary output signal to an 8-bit bus 44 and then to the D/A converter 42. (The sequencer 40 can be implemented as a 100 entry ROM look-up table that is addressed by a binary counter incremented by the clock.) The D/A converter converts the binary outputs from the sequencer into analog voltages, ranging from 0 volts (corresponding to a sequencer output of '00000000') to 4 volts (corresponding to a sequencer output of '11111111'.) The output from the D/A converter 42 is fed to the varactors 24, 30 in the antenna matching circuit 14 and causes that circuit to tune through its full range.

According to the teachings of Gaskill et al, to determine the optimum tuning condition, the control circuit 16 receives from the receiver subsystem 18 a Received Signal Strength Indicator (RSSI) signal which is indicative of received signal strength. An AGC signal is one example of a signal that can be used as the RSSI signal. The RSSI signal is applied to the input of an analog sample and hold circuit 46 and to one input of an analog comparator 50. The second input of the comparator is driven from a Max Hold output line 48 of the sample and hold circuit 46. These circuits cooperate to detect the optimum timing condition and store in a memory 54 the sequencer output that yielded that condition. See column 4, lines 35 to 68 of Gaskill et al.

It is respectfully submitted, however, that Gaskill et al does not disclose, teach, or suggest that the variable capacitor section includes capacitors and switching elements connected to the capacitors in series, as according to the present invention as recited in independent claims 1 and 11.

In addition, it is respectfully submitted that Gaskill et al does not disclose, teach, or suggest tuning for at least two frequencies. In this connection, it is noted that on page 7 of the Office Action the Examiner states that Gaskill et al as modified by Kianush et al discloses storing in a memory at least two sets of optimum bias voltage data for receiving radio waves having at least two frequencies. It is respectfully pointed out, however, that column 4, lines 42-55 of Gaskill et al cited by the Examiner merely teaches that the sequencer may have 100 states, each one providing a successively larger 8 bit 5 binary output signal to an 8-bit bus 44 and then to the D/A converter 42. And it is respectfully submitted that Gaskill et al does not disclose, teach or suggest storing data for setting on and off states of the switching elements to suitable combinations such that the radio wave receiver is in a predetermined reception state for each of at least two frequencies, as according to the claimed present invention.

In addition, Kianush et al merely discloses a structure in which plural capacitors are connected for selective tuning, and

it is respectfully submitted that Kianush et al does not at all disclose, teach, or suggest storing data for setting on and off states of switching elements to suitable combinations such that the radio wave receiver is in a predetermined reception state for each of at least two frequencies, as according to the claimed present invention.

Accordingly, it is respectfully submitted that even if the teachings of Gaskill et al and Kianush et al were combinable in the manner suggested by the Examiner, such combination would still fail achieve or render obvious the structure of the present invention whereby the memory is configured to store at least two items of data for setting a capacitance of the variable capacitor section to at least two suitable values that are suitable for receiving radio waves having at least two frequencies, as recited in amended independent claims 1 and 11.

Sakami et al, moreover, has merely been cited for the disclosure of an electronic timepiece radio in which the time signal is detected and the time indication is corrected by the detected time signal.

In summary, it is respectfully submitted that none of the cited references discloses, teaches or suggests storing data for setting on and off states of switching elements to suitable combinations for receiving radio waves having at least two

frequencies, as according to the present invention as recited in amended independent claims 1 and 11.

Accordingly, it is respectfully submitted that amended independent claims 1 and 11, and claims 3-5, 8-9, 13-15 and 18 respectively depending therefrom, clearly patentably distinguish over all of the cited prior art references, taken singly or in any combination, under 35 USC 102 as well as under 35 USC 103.

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In view of the foregoing, entry of this Amendment, allowance of the claims and the passing of this application to issue are respectfully solicited.

If the Examiner has any comments, questions, objections or recommendations, the Examiner is invited to telephone the undersigned for prompt action.

Respectfully submitted,

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